UNITED STATES PATENT APPLICATION

FOR

METHOD FOR PROVIDING CLOCK-NET AWARE DUMMY METAL USING DUMMY REGIONS

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METHOD FOR PROVIDING CLOCK-NET AWARE
DUMMY METAL USING DUMMY REGIONS

FIELD OF THE INVENTION

[01]   The present invention relates to methods for patterning dummy metal to achieve planarity for chemical-mechanical polishing of integrated circuits, and more particularly to a dummy fill software tool that provides clock-net aware dummy metal using dummy regions.

BACKGROUND OF THE INVENTION

[02]   Chemical Mechanical Polishing (CMP) is a part of the chip fabrication process that requires a uniform distribution of metal and silicon over the surface of the chip. To achieve this distribution, pieces of interconnect (metal or silicon) must be inserted into available spaces in low-density regions of the chip. This interconnect insertion is called dummy metal filling or simply dummy filling, and the inserted interconnect is called dummy metal.

[03]   Most fabrication processes require a minimum density for the interconnects on each layer of a multi-layer chip design. The interconnect density for a region is the sum total of the area of all interconnect in that region divided by the area of the region. Fabrication processes typically partition each layer of the design into rectangular regions, called tiles, and specify that the interconnect density of each tile meet a minimum density requirement.

[04]   The process of determining the number and placement of dummy metal is typically preformed by a dummy fill software tool after routing and timing closure during chip design flow. The dummy fill tool examines the tiles in each layer of the design and determines whether each tile has an interconnect density equal to or greater than the specified minimum density. If the interconnect density does not meet the minimum density, then the dummy fill tool inserts dummy metal in free regions of the tile.

[05]   Because dummy filling is one of the last steps in the chip design flow, it is important that the dummy metal is inserted into the chip in such a manner that minimizes any negative impact to timing. That is, patterning the dummy metal too close to signal nets increases capacitance between the dummy lines and the signal wires. The increased capacitance can affect the signal nets by slowing the transmission speed of signals, thereby degrading overall performance of the integrated circuit.

[06]   Therefore, a common goal of dummy filling techniques is the minimization of the parasitic capacitance introduced by the dummy metal. The parasitic capacitance introduced by a piece of dummy metal on a signal wire is inversely proportional to the distance between the two. This means that to minimize timing impact, dummy metal must be placed far away from signal nets.

[07]   Of signal nets, clock nets are of particular importance. Care must be taken to minimize the negative timing impact to clock nets. Traditionally, this has been achieved with a simplistic approach. The dummy fill tool is programmed to maintain a larger distance between wires of clock nets and the inserted dummy metal. This large dummy to clock distance is arrived at by studying the effect on timing that the inserted dummy metal has at various distances from clock nets in sample designs, and then hardcoding the distances into the dummy fill libraries for each type of process technology.

[08]   However, hardcoding a large "stay-away" distance between dummy metal and clock nets may lead to less available space in each tile for dummy metal insertion.   New process technologies increasingly demand higher minimum density values and more timing-aggresive designs. In this scenario, use of the simple large dummy-to-clock distance methodology is disadvantageous. This is because it is often impossible to insert enough dummy metal into a tile to meet the required minimum density without reducing the large dummy-to-clock distance.   In this case, traditional metal-fill tools complete their run without reaching minimum density in some tiles, requiring a second run of the tool for the problematic tiles in which the dummy-to-clock distance is reduced. If there is more than one such tile requiring a rerun, and the dummy fill tool can handle only one tile at a time, multiple runs may be needed: one for each tile.   Such an involved, iterative process can significantly impact the design schedule.

[09]   Accordingly what is needed is an algorithm for dummy fill that minimizes the negative timing impact of dummy metal on clock nets, while at the same time achieving minimum density in a single run. The present invention addresses such a need.

SUMMARY OF THE INVENTION

[010]   The present invention provides a method for inserting dummy metal into a circuit design, which includes a plurality of objects and clock nets. Aspects of the invention include identifying free spaces on each layer of the chip design suitable for dummy metal insertion, wherein the free spaces are referred to as dummy regions. . Thereafter, the dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last. In a preferred embodiment, the dummy regions are further prioritized such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

[011]   According to the method and system disclosed herein, inserting dummy metal into dummy regions that are not adjacent to clock nets prior to inserting dummy metal into clock-net adjacent dummy regions will be sufficient to meet the minimum density requirement. This means that in many cases, no dummy metal (or a minimal amount) is inserted in the clock-net adjacent dummy regions, thereby minimizing the timing impact to the adjacent clock nets.

BRIEF DESCRIPTION OF THE DRAWINGS

[012]   Figure 1 is a block diagram illustrating a software and hardware environment in which the present invention may be implemented.

[013]   Figure 2 is a flow diagram illustrating the process performed by the dummy fill application for inserting dummy metal into the chip design during a free space finding phase.

[014]   Figure 3 is a diagram showing the handling of the dummy regions in a tile after all objects in the database have been iterated over.

[015]   Figure 4 is a diagram illustrating the properties stored for each tile.

[016]   Figure 5 is a flow diagram illustrating the process performed by the dummy fill application during a dummy metal insertion phase.

[017]   Figure 6 is a diagram illustrating metal insertion in clock-net adjacent dummy regions according to preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[018]   The present invention relates to design methodologies for dummy metal filling. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent

application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

[019]   The present invention provides a software tool for dummy metal filling of a chip design during the design phase. Figure 1 is a block diagram illustrating a software and hardware environment in which the present invention may be implemented. The dummy fill software application 12 is preferably executed on a computer 14, which may be a workstation or a server. The dummy fill application 12 accesses a design database 16, which includes information describing all objects of a fully routed integrated circuit design, such as cells, interconnects, and signal nets. In a preferred environment, each layer of the chip is partitioned into tiles, each equal in size to a process-specified tile-size. The design database 16 also includes the minimum density requirement for the tiles. The dummy fill application 12 is one of many design flow tools, and is primarily invoked after routing and timing closure stages of a design flow.

[020]   According to the present invention, the dummy fill application 12 inserts dummy metal into the chip design in a manner that minimizes the timing impact to clock nets, while the same time achieving the minimum density requirement in a single run. The dummy fill application 12 operates in two phases. In the first

phase, referred to as the free-space finding phase, the dummy fill application 12 searches each layer of the chip design for empty spaces suitable for dummy metal insertion. These empty spaces are referred to herein as dummy regions.

[021] In the second phase, referred to as the dummy metal insertion phase, the dummy fill application 12 inserts a sufficient amount of dummy metal into the dummy regions discovered in the first phase to meet the minimum density requirement of each tile, but prior to doing so, prioritizes the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last. And, as further described below, the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions adjacent to narrower clock nets.

[022] By prioritizing the empty spaces in this manner, the minimum density requirements of the chip can be met, while minimizing negative impact to the clock nets because the distance between the dummy metal and clock nets, especially the thicker, more important clock nets, is maximized.

[023] Figure 2 is a flow diagram illustrating the process for inserting dummy metal into the chip design performed by the dummy fill application 12 during the free space finding phase. The free space finding phase begins in step 200 by initializing a series of properties for each tile, including a dummy region list, interconnect area, and dummy metal area. The dummy regions are a list of free

areas in the tile suitable for dummy metal. In a preferred embodiment, the dummy region list for each tile is initialized with a single rectangle corresponding to the outline of the tile. The interconnect area property will be used to specify the total amount of interconnect area included in the tile, and the dummy metal area property will be used to specify the total amount of dummy metal inserted into the tile.

[024] In step 202, the dummy fill application 12 traverses the design database 16 and for each object found in the current tile, subtracts the outline of the object from the dummy region on which it lies.

[025] Figure 3 is a diagram showing the processing of a dummy region 50 once an object 52 is found intersecting the dummy region 50. Referring to both Figures 2 and 3, the area of the object 52 is added to the interconnect area property for the tile in step 204. In step 206, the current dummy region is partitioned into up to four sub-dummy regions 50a-50d around the subtracted area. In a preferred embodiment, each sub-dummy region 50a-50d is formed between one of the edges of the object 52 and the corresponding edge of the current dummy region 50. Therefore, if the object 52 is located along one edge of the original dummy region 50, then only three sub-dummy regions 50a-50c will be created. In step 208, the original dummy region 50 is removed from the dummy list and the new dummy regions 54 are inserted into the list. The result

of this process is a list of dummy regions 50 that represent free spaces in the tile suitable for dummy metal.

[026] According to the present invention, objects in the design database 16 representing wires on clock nets are treated specially. If it is determined in step 210 that the current object is a wire on a clock net, then in step 212, the width of the wire is stored as a clock net width property of the region 50 created by its outline. Also, the sub-dummy regions 50a - 50c located immediately adjacent to the clock net wire are tagged with a clock net edge property as well as the clock net width property in step 214 so as to be identifiable later. The sub-dummy regions 50a - 50c replace their parent (50) on the dummy list.

[027] In step 216, it is determined if the current tile includes additional objects, and if so, the database traversal continues.

[028] Figure 4 is a diagram illustrating the properties stored for each tile after all the objects have been found. The properties include the dummy region list 60, the tile area 62, the interconnect area 64, and the dummy metal area 66. Also maintained for each clock net region is a timing factor 72, which is calculated during the second phase. In addition, several properties may also be maintained for each of the dummy regions 50 in the dummy region list 60 including a clock net edge 70 property, which identifies the region as being adjacent to a clock net,

and a clock net width 68 property, which identifies the width of the adjacent clock net wire.

[029]   Referring again to Figure 2, according to one aspect of the present invention, the dummy metal area 66 that needs to be inserted to meet minimum density is calculated in step 218 for the current tile is as follows:

[030]   Dummy Metal Area = (Minimum Density * Tile Area) - Interconnect Area

[031]   In step 220, it is determined whether there are more tiles to process. If there are more tiles, the process continues. Otherwise, the free space finding phase is complete and the dummy fill application 12 executes the dummy metal insertion phase.

[032]   Figure 5 is a flow diagram illustrating the process performed by the dummy fill application 12 during the dummy metal insertion phase. The dummy metal insertion phase begins in step 250 in which the timing factor 72 is calculated for each dummy region 50 in the list 60 that has a clock net width 68 property. The timing factor 72 attempts to capture the timing criticality of a dummy region 50. In a clock tree, the width of a wire is indicative of its order in a hierarchy. A wide wire is likely to be supplying current to more branches than a thinner wire, and is therefore more timing critical.

[033] In a preferred embodiment, the timing factor 72 is calculated using the formula:

[034] Timing Factor = Clock Net Width * Clock Net Criticality

[035] According to one aspect of the present invention, the clock net criticality is an integral value that the user can specify to control the timing factor 72 assigned to the dummy regions. In a preferred embodiment, the criticality factor is assigned to the entire clock net and is inherited by all wires on that clock net. Also in a preferred embodiment, the clock net criticality values are stored in the form of lookup table in file and provides the user control over relative treatment of clock nets. More critical clock nets can be given higher values. In the absence of a user-specified value, the clock net criticality for a clock net is assigned some default value, e.g., '1'.

[036] The table below illustrates an example Clock Net Criticality Lookup table:

Clock Nets	Clock Net Criticality
Clock_Net_A	2
Clock_Net_B	3
I	I

[037] In a preferred embodiment, all dummy regions 50 not adjacent to a clock-net wire are assigned a Timing Factor of 0.

[038] Referring again to Figure 5, after the timing factors 72 have been calculated in step 252, the dummy region list 60 for each tile is sorted in ascending order of the timing factor 72. According to the present invention, this establishes a prioritization for the dummy regions 50 in which dummy regions 50 adjacent to clock nets are placed on the list 60 after dummy regions 50 that are not adjacent to clock nets. Within the sub-list of clock-net adjacent dummy regions 50, the dummy regions 50 adjacent to wider wires of a clock net are listed after the dummy regions 50 adjacent to narrower wires of the same clock net. Between two dummy regions 50 adjacent to clock net wires of the same width, the dummy region 50 that is adjacent to a net having a higher criticality value is listed after the other.

[039] After the sorting, the dummy that application 12 in step 254, begins inserting dummy metal into the sorted dummy regions 50, starting with the first dummy region 50 on the list. After each insertion, the inserted area is added to the interconnect area 64 property of the tile in step 256, and the dummy metal area 66 for the tile is recalculated in step 258.

[040] This process is continued in step 260 until the dummy metal area 66 becomes negative. Thereafter, the process continues with the next tile in step 262 until all tiles are processed.

[041] In most cases, the value for the dummy metal area 66 will become negative before traversal of the dummy region list 60 reaches the clock-net adjacent dummy

regions 50. This means that in many cases, no dummy metal (or a minimal amount) is inserted in the clock-net adjacent dummy regions 50, thereby minimizing the timing impact to the adjacent clock nets.

[042] If metal insertion is required in any of the clock-net adjacent dummy regions 50, then the metal insertion may be performed starting with the edge opposite the clock-net adjacent edge, using the clock net edge 70 property. FIG. 6 is a diagram showing the insertion of dummy metal in a clock-net adjacent dummy region, starting with the edge opposite to the one identified by the clock net edge 70 property. According to this aspect of the present invention, if the value for the dummy metal area 66 becomes negative before the clock-net adjacent dummy region 50 is completely filled, the spacing between the dummy metal 80 and the clock net wire 82 is the maximum possible.

[043] A dummy fill application 12 has been described that provides a simple and efficient method for dummy metal insertion that minimizes the timing impact to clock nets and at the same time guarantees reaching minimum density in a single pass.

[044] The present invention has been described in accordance with the embodiments shown, and one of ordinary skill in the art will readily recognize that there could be variations to the embodiments, and any variations would be within the spirit and scope of the present invention. Accordingly, many modifications may

be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.